WAFER LEVEL BURN-IN AND ELECTRICAL TEST SYSTEM AND METHOD

ABSTRACT OF THE DISCLOSURE

A burn-in and electrical test system (20) includes a temperature controlled zone (22) and a cool zone (24) separated by a transition zone 25. The temperature controlled zone (22) is configured to receive a plurality of wafer cartridges (26) and connect the cartridges (26) to test electronics (28) and power electronics (30), which are mounted in the cool zone (24). Each of the wafer cartridges (26) contains a semiconductor wafer incorporating a plurality of integrated circuits. The test electronics (28) consists of a pattern generator PCB (100) and a signal driver and fault analysis PCB (102) connected together by a parallel bus (104). The pattern generator PCB (100) and the fault analysis PCB (102) are connected to a rigid signal probe PCB (104) in cartridge (26) to provide a straight through signal path. The probe PCB (104) is rigid in order to allow close control of capacitance between each signal line and a backplane, thus providing impedance controlled interconnections between a semiconductor wafer under test and the test electronics (28). The power distribution system (30) is connected to a probe power PCB (106) in the cartridge (26). The probe power PCB (106) has at least a bendable portion in order to allow it to be positioned closely adjacent to and parallel with the rigid probe PCB (104), yet extend a substantial distance away from the probe PCB (106) at its interconnection (109).